FIG. 1

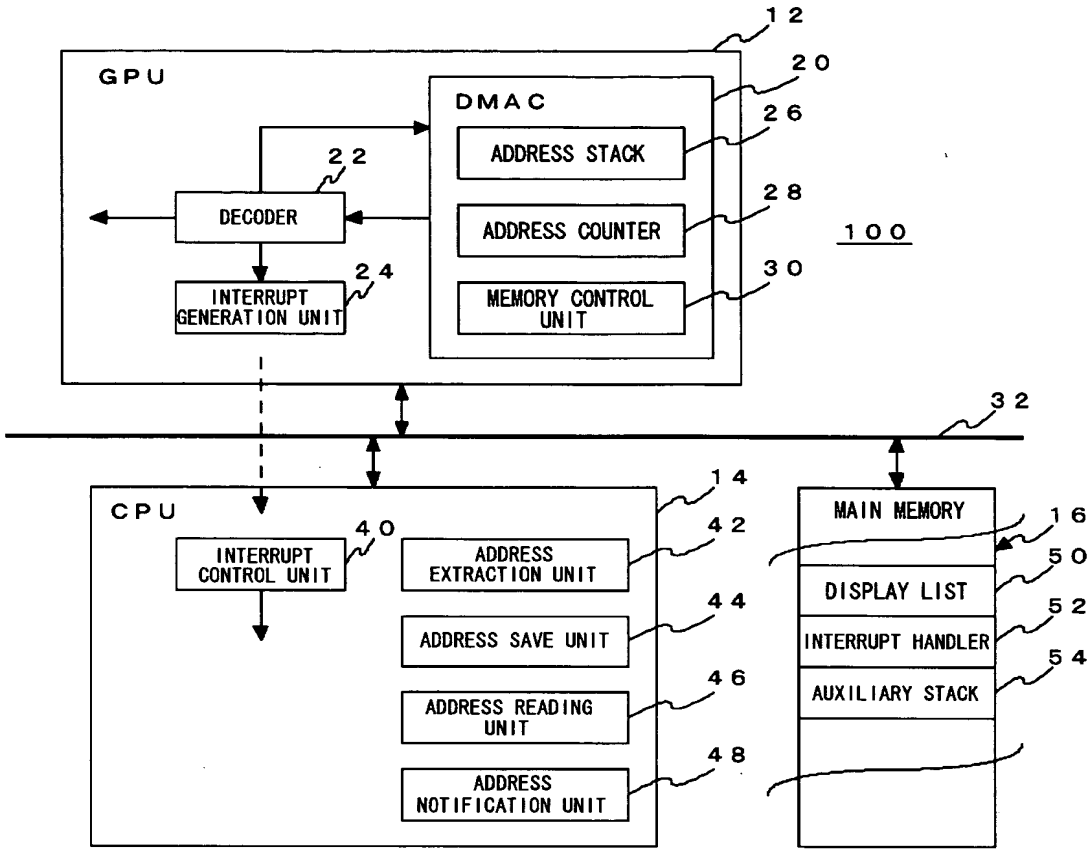

12
GPU
20
DMAC
26
ADDRESS STACK
22
DECODER
28
ADDRESS COUNTER
100
24
INTERRUPT GENERATION UNIT
30
MEMORY CONTROL UNIT
32
14
CPU
40
INTERRUPT CONTROL UNIT
42
ADDRESS EXTRACTION UNIT
44
ADDRESS SAVE UNIT
46
ADDRESS READING UNIT
48
ADDRESS NOTIFICATION UNIT
MAIN MEMORY
16
50
DISPLAY LIST
52
INTERRUPT HANDLER
54
AUXILIARY STACK

FIG. 2

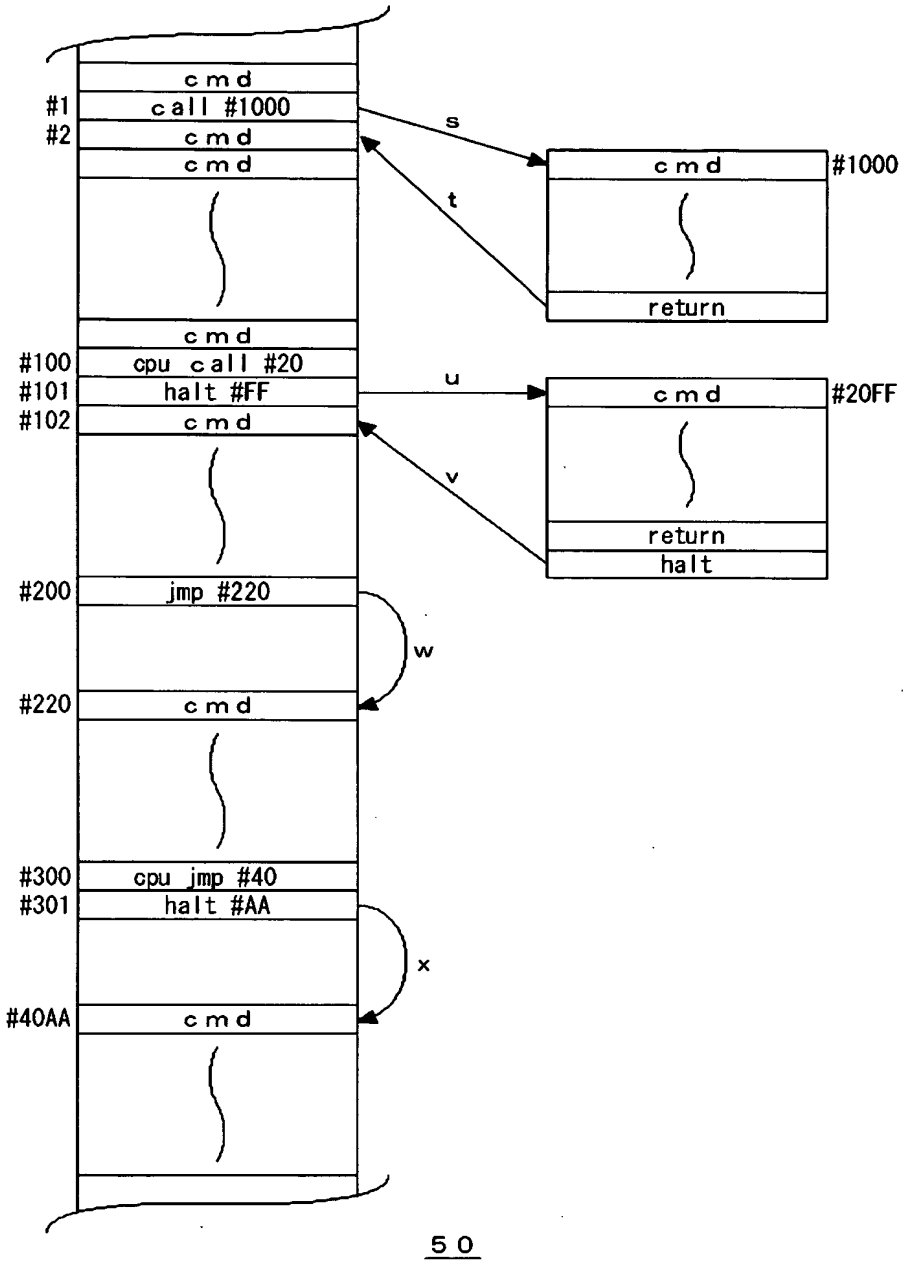


FIG. 3

	31	23	15	0
cpu call	E 1	0 1	addr 16-31	
halt	E 2	—	addr 0-15	

FIG. 4

	31	23	15	0
cpu jmp	E 1	0 0	addr 16-31	
halt	E 2	—	addr 0-15	

FIG. 5

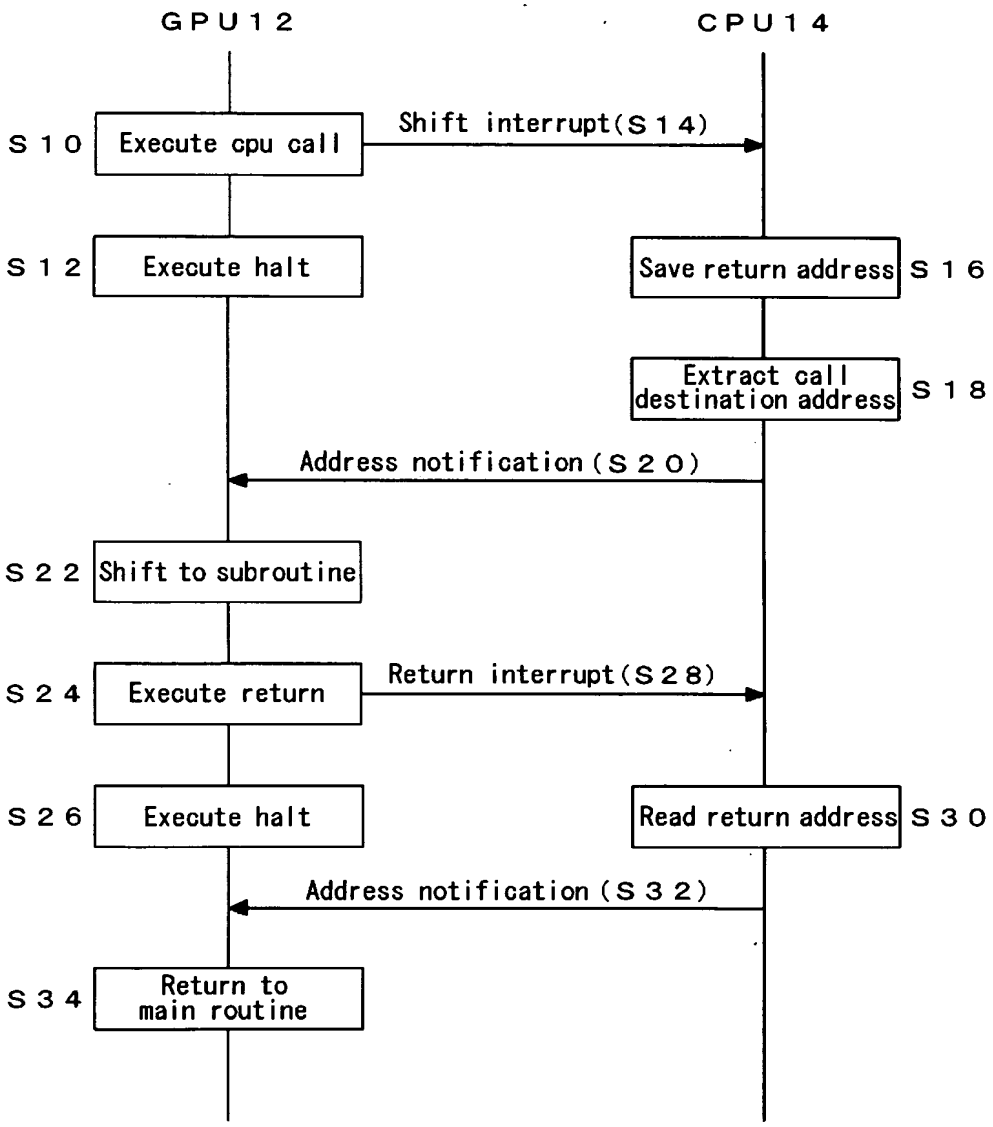
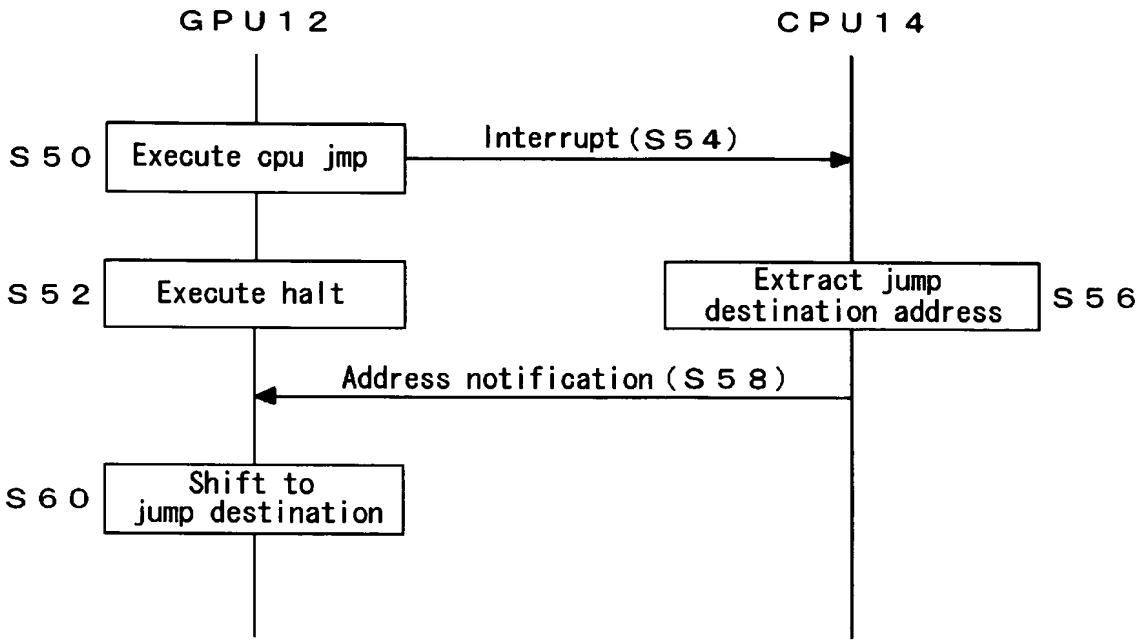


FIG. 6


GPU12
CPU14
S50
Execute cpu jmp
Interrupt (S54)
S52
Execute halt
Extract jump destination address
S56
Address notification (S58)
S60
Shift to jump destination